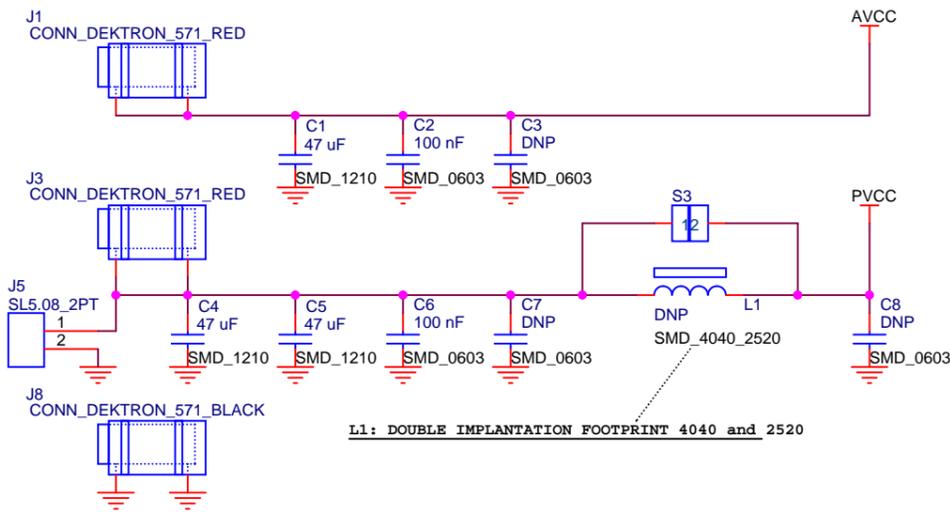
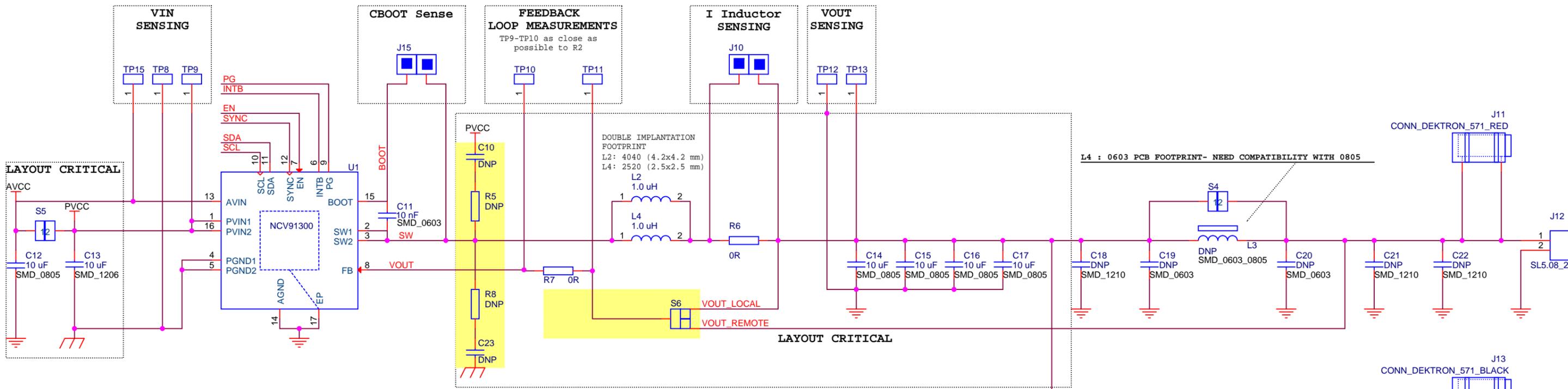
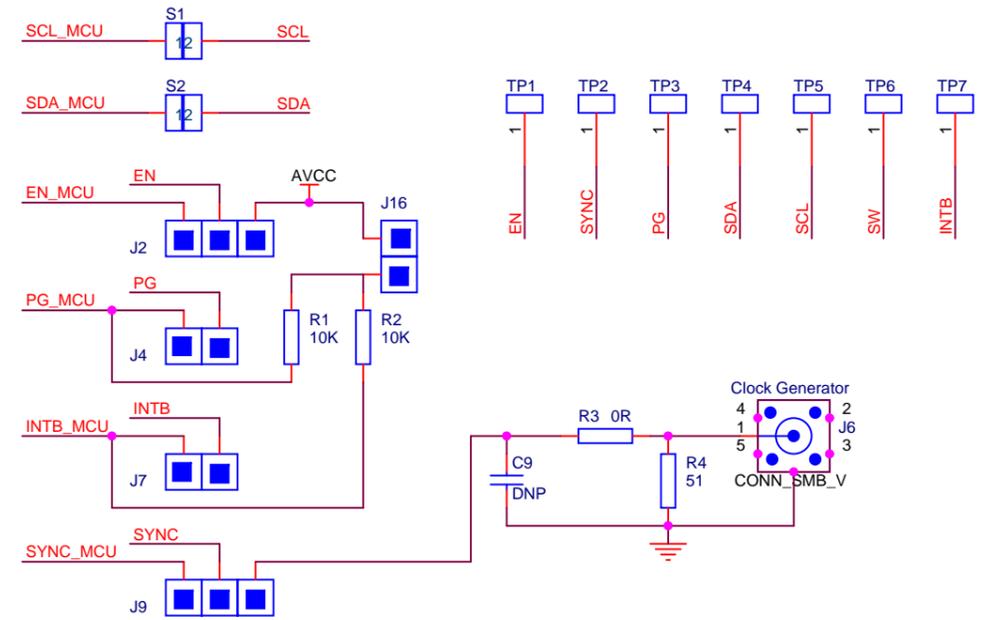
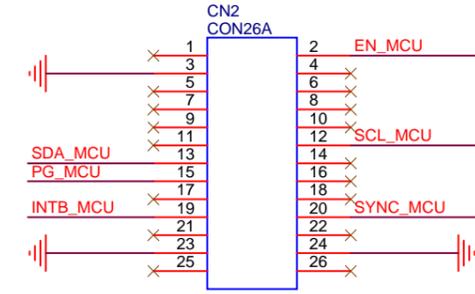
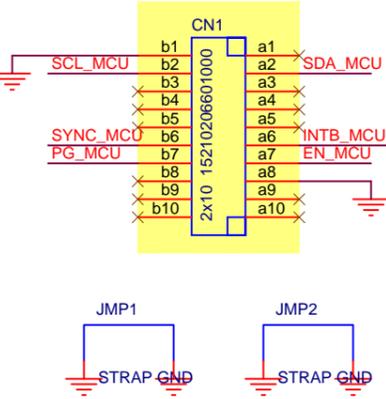


INPUT POWER CONNECTORS

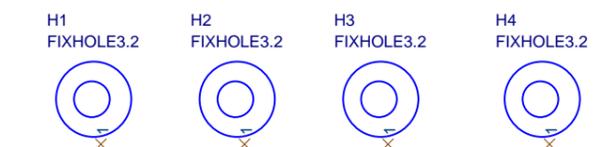
PVCC	NCV91300 Power Input (2.0 ~ 5.5 V)
AVCC	NCV91300 Analog Input (3.0 ~ 5.5 V)



TEST POINTS - CONNECTORS



AGND and PGND Connected in one point

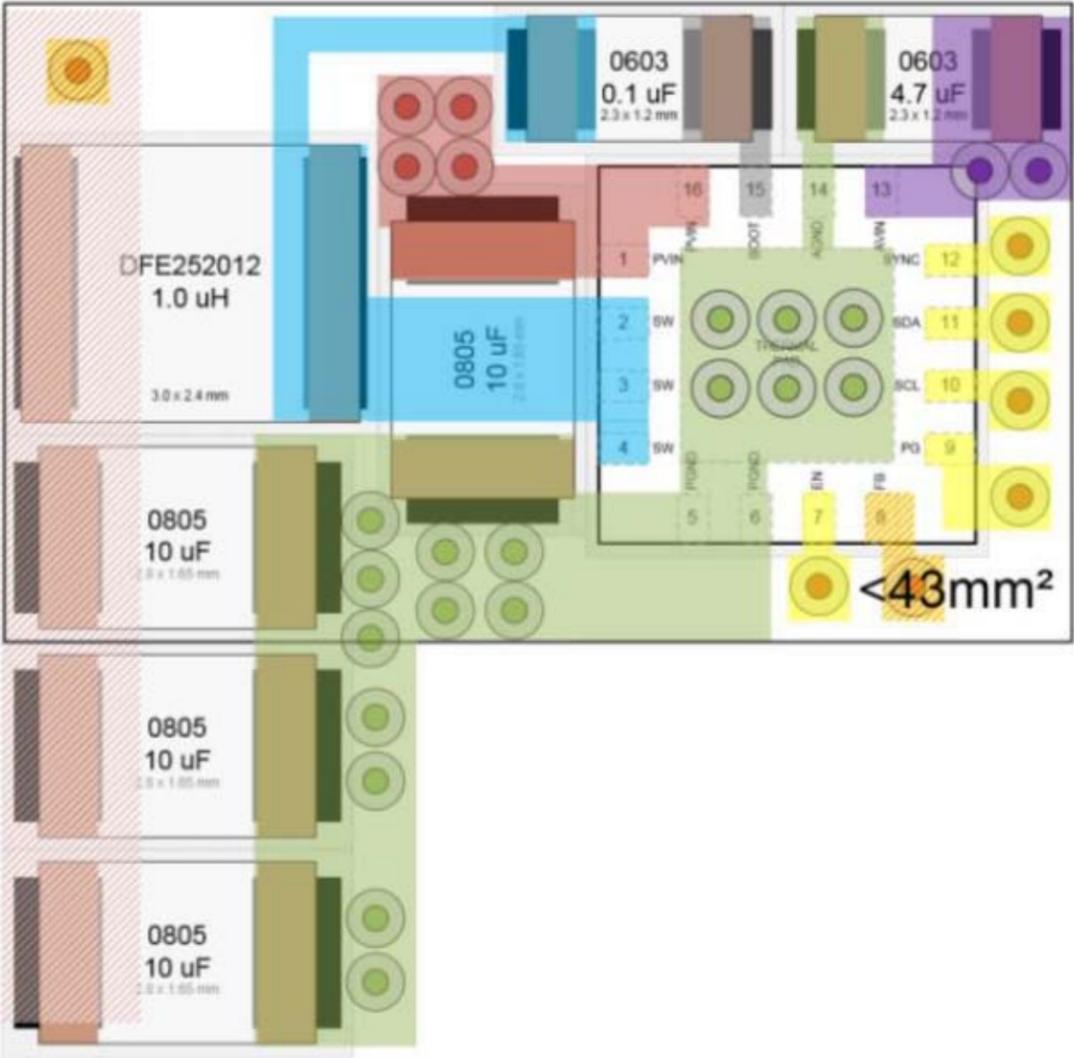


Components placed in bottom

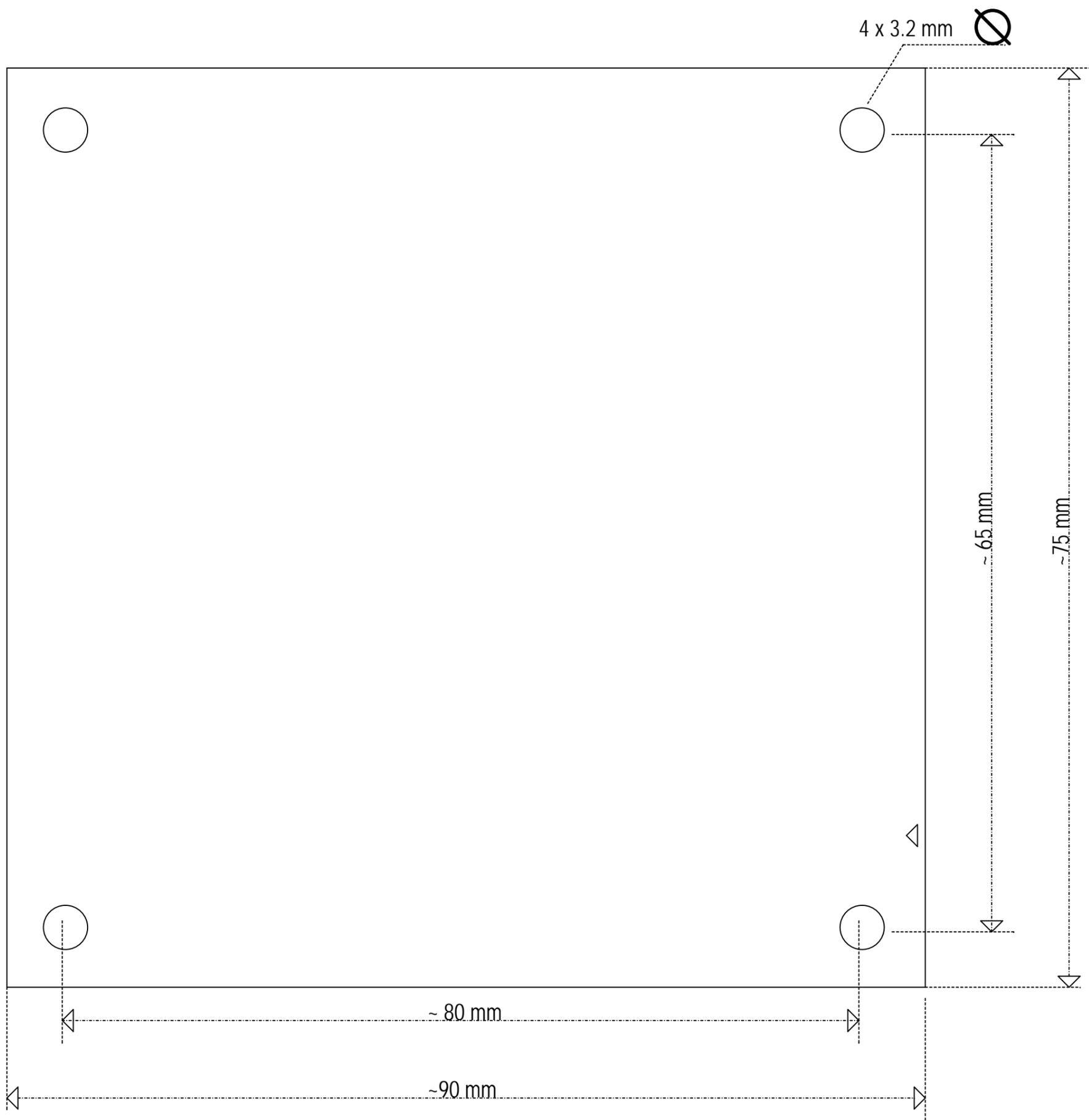
REV	DATE	DESCRIPTION	AUTHOR
B0	06/07/18	Add AVIN test point, CBOOT sense + GND to Q1...	PDE
A3	29/05/18	Add possibility to short AVIN and PVIN, remove inductor test points	PDE
A2	16/05/18	Add the 2 points strap for current sensing	PDE
A1	26/03/18	New pinout version (with 2 sw)	GMA
A0	06/12/17	Initial Version	PDE

Designed by PDE	ON SEMICONDUCTOR 132 Chemin Basso Cambo BP53512 31035 TOULOUSE Cedex 1 France	
NCV91300 QFN16 DEMO BOARD REV B		Rev B0
DWG NO TLS-P-002-B-0718-PDE		
Thursday, November 15, 2018	Scale	Size A3
Sheet 1 of 3		

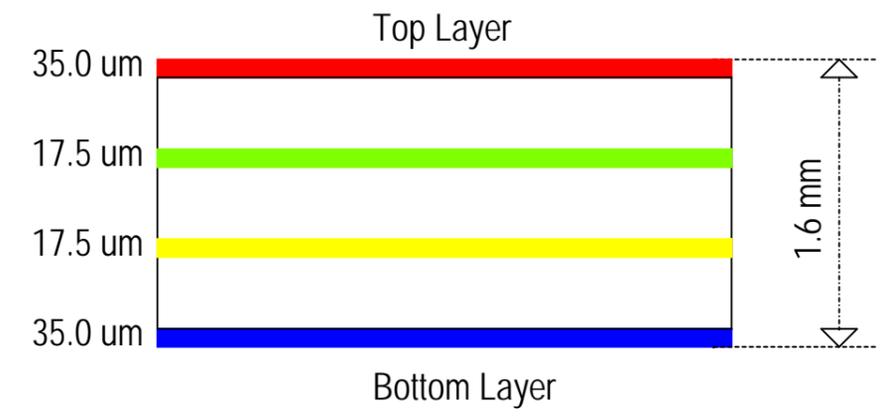
Example / Approach about Layout Implementation



A0	06/12/17	Initial Version	PhA
REV	DATE	DESCRIPTION	AUTHOR
Designed by PhA	ON SEMICONDUCTOR 132 Chemin Basso Cambo BP53512 31035 TOULOUSE Cedex 1 France		 ON Semiconductor
		NCV91300 QFN16 DEMO BOARD REV A	Rev A2
		DWG NO TLS-P-002-A-0518-PDE	
Thursday, November 15, 2018	Scale	Size A3	Sheet 2 of 3



Layer Structure



A0	06/12/17	Initial Version	PhA
REV	DATE	DESCRIPTION	AUTHOR
Designed by PhA	ON SEMICONDUCTOR 132 Chemin Basso Cambo BP53512 31035 TOULOUSE Cedex 1 France		 ON Semiconductor
		NCV91300 QFN16 DEMO BOARD REV A	Rev A2
		DWG NO TLS-P-002-A-0518-PDE	
Thursday, November 15, 2018		Scale	Size A3 Sheet 3 of 3